WHAT IS CLAIMED IS:

1. A thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate with a display area and a peripheral area surrounding the display area, the peripheral area having an upper region above the display area and a lower region below the display area;

signal lines formed on the substrate such that the signal lines are bundled into a plurality of blocks, each block having a predetermined number of signal lines;

a plurality of first upper repair lines formed at the upper peripheral region of the substrate, crossing one or more blocks of the signal lines;

a plurality of second upper repair lines formed at the upper peripheral region of the substrate, crossing all of the signal lines;

a plurality of first lower repair lines formed at the lower peripheral region of the substrate, connected to the corresponding first upper repair lines, the first lower repair lines crossing the signal lines crossed by the first upper repair lines;

a plurality of second lower repair lines formed at the lower peripheral region of the substrate, crossing all of the signal lines;

a plurality of upper connection members crossing the first upper repair lines and the second upper repair lines; and

a plurality of lower connection members crossing the first lower repair lines and the second lower repair lines.

2. The thin film transistor array substrate of claim 1, further

comprising:

a plurality of first interconnection lines interconnecting the first upper repair lines and the first lower repair lines.

3. The thin film transistor array substrate of claim 2, wherein the first upper repair lines are drawn from two or more dummy pins of integrated circuits for driving the signal lines, and are linked to the first interconnection lines.

4. The thin film transistor array substrate of claim 2, further comprising:

a plurality of second interconnection lines interconnecting the first upper repair lines and the first lower repair lines.

5. The thin film transistor array substrate of claim 1, further comprising:

a plurality of third upper repair lines formed at the upper peripheral region of the substrate while crossing the upper connection members and all of the signal lines; and

a plurality of third lower repair lines formed at the lower peripheral region of the substrate while crossing the lower connection members and all of the signal lines.

6. The thin film transistor array substrate of claim 1, wherein each block of the signal lines comprises the signal lines connected to one of the integrated circuits.

7. The thin film transistor array substrate of claim 6, wherein the first upper and lower repair lines cross two blocks of the signal lines.

8. The thin film transistor array substrate of claim 7, wherein one or more of the upper and lower connection members are formed at each block of the signal lines.

9. The thin film transistor array substrate of claim 4, wherein the first and second interconnection lines are formed on a printed circuit board.

10. The thin film transistor array substrate of claim 4, further comprising:

a signal amplifying circuit in the first and second interconnection lines.